L Number	Hits	Search Text	DB	Time stamp
13	3315	ball with bonding	USPAT; US-PGPUB	2002/08/28 15:59
14	1662	(ball with bonding) and pad and wire	USPAT; US-PGPUB	2002/08/28 15:59
15	230	((ball with bonding) and pad and wire) and (deform$5 with wire)	USPAT; US-PGPUB	2002/08/28 15:59
16	198	(((ball with bonding) and pad and wire) and (deform$5 with wire)) and @ad<=20010322	USPAT; US-PGPUB	2002/08/28 15:40
17	3013	ball with bonding	EPO; JPO; DERWENT; IBM_TDB	2002/08/28 15:59
18	607	(ball with bonding) and pad and wire	EPO; JPO; DERWENT; IBM_TDB	2002/08/28 15:59
19	15	((ball with bonding) and pad and wire) and (deform$5 with wire)	EPO; JPO; DERWENT; IBM_TDB	2002/08/28 16:00

L Number	Hits	Search Text	DB	Time stamp
1	60	base and (die adj pad) and encapsulat$4 and ball and bonding	USPAT; US-PGPUB	2002/08/28 17:13
2	55	(base and (die adj pad) and encapsulat$4 and ball and bonding) and @ad<=20010322	USPAT; US-PGPUB	2002/08/28 17:13

mounted, a heat sink 30, a plurality of lead terminals 12b, a plurality of wires W, and package resin 22.

(83) The resin-packaged semiconductor device 10 is manufactured by using a leadframe 12, wherein the **die pad** 12a and the lead terminals 12b are provided on the leadframe 12. Although a method for manufacturing the resin-package semiconductor device 10 is stated later, the **die pad** 12a is formed by a thin-walled metal sheet such as of copper, for example, in a rectangular form as viewed in plan. The lead terminals 12b are formed from a thin-walled metal sheet such as of copper similarly to the **die pad** 12a, and each comprise an inner lead 12g embedded within the package resin 22 and an outer lead 12h projecting outward from the package resin 22. The lead terminals 12b are for mounting the resin-packaged semiconductor device 10 on a desired position. Specifically, the resin-packaged semiconductor device 10 is placed on an area applied with a solder cream in a manner contacted by the lead terminals 12b, and then the solder cream is heated to cause solder reflow. Thus, the resin-packaged semiconductor device 10 can be surface-mounted on that area.

(84) The first semiconductor chip 14 and the second semiconductor 16 are structured, for example, as an LSI chip or other IC chips, and have one surface on which desired electronic circuits (circuit elements) are fabricated integral therewith. Consequently, the surfaces of the first semiconductor chip 14 and the second semiconductor chip 16 are active surfaces fabricated with electronic circuits, while the backsides, i.e., the back surfaces of the silicon chips having no electronic circuits, are passive surfaces. The first semiconductor

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☒	JP 10056032 A	19980224	8
2	☐	☒	JP 05299459 A	19931112	5
3	☐	☒	JP 10056032 A	19980224	8

	Title	Current OR	Current XRef
1	SEMICONDUCTOR DEVICE		
2	SEMICONDUCTOR DEVICE		
3	Semiconductor device - has inner lead whose height is set almost equal to that of wire bonding ball		

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		OSHIDA, IWAO	☒	☐	☐	☐	☐	☐	☐
2		AOYANAGI, HITOSHI et al.	☒	☐	☐	☐	☐	☐	☐
3			☒	☐	☐	☐	☐	☐	☐

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1	JP 10056032 A	☐
2	JP 05299459 A	☐
3	JP 10056032 A	☐

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☒	US 20020068426 A1	20020606	30
2	☐	☒	US 20010035575 A1	20011101	63
3	☐	☒	US 20010023534 A1	20010927	10
4	☐	☒	US 20010020635 A1	20010913	14
5	☐	☒	US 20010020546 A1	20010913	155
6	☐	☒	US 20010002726 A1	20010607	26
7	☐	☒	US 6426563 B1	20020730	16
8	☐	☒	US 6420256 B1	20020716	8
9	☐	☒	US 6413797 B2	20020702	25
10	☐	☒	US 6336269 B1	20020108	131
11	☐	☒	US 6267290 B1	20010731	8

	Title	Current OR	Current XRef
1	Microelectronic packages having deformed bonded leads and methods therefor	438/616	257/784; 438/617
2	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	257/690	257/692; 257/696; 257/701; 257/723; 257/737; 257/738
3	Bent wire forming method	29/843	29/860; 29/868
4	Electronic part mounting method	228/180.5	228/170; 228/173.1; 228/206
5	Electrical contact structures formed by configuring a flexible wire to have a springable shape and overcoating the wire with at least one layer of a resilient conductive material, methods of mounting the contact structures to electronic components, and applications for employing the contact structures	174/261	174/24; 174/255
6	Semiconductor device and method for making the same	257/678	
7	Semiconductor device and method for manufacturing the same	257/780	257/781; 257/782; 257/784; 257/786
8	Method of improving interconnect of semiconductor devices by using a flattened ball bond	438/613	438/123; 438/617
9	Semiconductor device and method for making the same	438/108	438/107; 438/109
10	Method of fabricating an interconnection element	29/885	228/180.5; 228/199; 29/825; 29/830; 29/840; 29/843
11	Control of size and heat affected zone for fine pitch wire bonding	228/180.5	228/1.1; 228/110.1; 228/4.5

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		Fjelstad, Joseph et al.	☒	☐	☐	☐	☐	☐	☐
2		MIYAZAKI, CHUICHI et al.	☒	☐	☐	☐	☐	☐	☐
3		Tamai, Hideaki et al.	☒	☐	☐	☐	☐	☐	☐
4		Maeda, Yukihiro et al.	☒	☐	☐	☐	☐	☐	☐
5		Eldridge, Benjamin N. et al.	☒	☐	☐	☐	☐	☐	☐
6		Oka, Hiroshi et al.	☒	☐	☐	☐	☐	☐	☐
7		Fujihira, Mitsuaki	☒	☐	☐	☐	☐	☐	☐
8		Ball, Michael B.	☒	☐	☐	☐	☐	☐	☐
9		Oka, Hiroshi et al.	☒	☐	☐	☐	☐	☐	☐
10		Eldridge, Benjamin N. et al.	☒	☐	☐	☐	☐	☐	☐
11		Murdeshwar, Nikhil M.	☒	☐	☐	☐	☐	☐	☐

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1	US 20020068426	☐
2	US 20010035575	☐
3	US 20010023534	☐
4	US 20010020635	☐
5	US 20010020546	☐
6	US 20010002726	☐
7	US 6426563	☐
8	US 6420256	☐
9	US 6413797	☐
10	US 6336269	☐
11	US 6267290	☐

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12	☐	☒	US 6252175 B1	20010626	24
13	☐	☒	US 6192578 B1	20010227	16
14	☐	☒	US 6169331 B1	20010102	18
15	☐	☒	US 6110823 A	20000829	130
16	☐	☒	US 6034440 A	20000307	10
17	☐	☒	US 5842628 A	19981201	33
18	☐	☒	US 5821627 A	19981013	46
19	☐	☒	US 5773311 A	19980630	8
20	☐	☒	US 4976393 A	19901211	20

	Title	Current OR	Current XRef
12	Electronic assembly comprising a substrate and a plurality of springable interconnection elements secured to terminals of the substrate	174/250	174/257; 361/769; 361/771; 361/774; 361/776; 439/876; 439/886; 439/887
13	Method for electrically coupling bond pads of a microelectronic device	29/840	228/1.1; 228/4.5; 29/832
14	Apparatus for electrically coupling bond pads of a microelectronic device	257/784	257/666; 257/690; 257/691; 257/693; 257/723; 257/772; 257/776; 257/779; 257/780; 257/786
15	Method of modifying the thickness of a plating on a member by creating a temperature gradient on the member, applications for employing such a method, and structures resulting from such a method	438/660	438/14; 438/597; 438/612
16	Method of improving interconnect of semiconductor devices by utilizing a flattened ball bond	257/786	257/758; 257/780; 257/784
17	Wire bonding method, semiconductor device, capillary for wire bonding and ball bump forming method	228/180.5	219/56.22
18	Electronic circuit device	257/780	257/737; 257/765; 257/781
19	Method for providing a test connection and a permanent connection site on an unpackaged semiconductor die	438/15	228/103; 29/593; 438/617
20	Semiconductor device and production process thereof, as well as wire bonding device used therefor	228/111	219/56.21; 228/180.5; 228/220

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
12		Khandros, Igor Y.	☒	☐	☐	☐	☐	☐	☐
13		Manning, Troy A. et al.	☒	☐	☐	☐	☐	☐	☐
14		Manning, Troy A. et al.	☒	☐	☐	☐	☐	☐	☐
15		Eldridge, Benjamin N. et al.	☒	☐	☐	☐	☐	☐	☐
16		Ball, Michael B.	☒	☐	☐	☐	☐	☐	☐
17		Nomoto, Ryuji et al.	☒	☐	☐	☐	☐	☐	☐
18		Mori, Miki et al.	☒	☐	☐	☐	☐	☐	☐
19		Cullinan, Deborah A. et al.	☒	☐	☐	☐	☐	☐	☐
20		Nakajima, Makoto et al.	☒	☐	☐	☐	☐	☐	☐

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12	US 6252175	☐
13	US 6192578	☐
14	US 6169331	☐
15	US 6110823	☐
16	US 6034440	☐
17	US 5842628	☐
18	US 5821627	☐
19	US 5773311	☐
20	US 4976393	☐

	U	1 [1]	Document ID	Issue Date	Pages
1	☐	☒	US 20010053448 A1	20011220	20
2	☐	☒	US 6410987 B1	20020625	68
3	☐	☒	US 6373127 B1	20020416	10
4	☐	☒	US 6372351 B1	20020416	11
5	☐	☒	US 6225418 B1	20010501	18
6	☐	☒	US 6133637 A	20001017	50
7	☐	☒	US 5969426 A	19991019	25

	Title	Current OR	Current XRef
1	Thermosetting resin composition	428/447	
2	Semiconductor device and a method of manufacturing the same and an electronic device	257/777	257/676; 257/684; 257/685; 257/686; 257/690; 257/691; 257/692; 257/723; 257/784; 361/813
3	Integrated capacitor on the back of a chip	257/676	257/666; 257/691; 257/707; 257/719; 257/784; 361/723; 361/734
4	Encapsulant epoxy resin composition and electronic device	428/416	428/620; 523/440; 523/468
5	Thermosetting resin composition	525/524	257/738; 257/783; 427/386; 427/387; 428/447; 525/476; 528/10; 528/27; 528/32; 528/38; 528/418; 528/421; 549/215; 549/512; 556/438
6	Semiconductor device having a plurality of semiconductor chips	257/777	257/666; 257/686; 257/778; 257/779; 257/784; 257/795; 438/108; 438/109
7	Substrateless resin encapsulated semiconductor device	257/778	257/666; 257/676; 257/690; 257/787

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		Satsu, Yuichi et al.	☒	☐	☐	☐	☐	☐	☐
2		Kanemoto, Kouichi et al.	☒	☐	☐	☐	☐	☐	☐
3		Baudouin, Daniel et al.	☒	☐	☐	☐	☐	☐	☐
4		Takemiya, Keizo et al.	☒	☐	☐	☐	☐	☐	☐
5		Satsu, Yuichi et al.	☒	☐	☐	☐	☐	☐	☐
6		Hikita, Junichi et al.	☒	☐	☐	☐	☐	☐	☐
7		Baba, Shinji et al.	☒	☐	☐	☐	☐	☐	☐

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1	US 20010053448	☐
2	US 6410987	☐
3	US 6373127	☐
4	US 6372351	☐
5	US 6225418	☐
6	US 6133637	☐
7	US 5969426	☐

	U	1 [1]	Document ID	Issue Date	Pages
8	☐	☒	US 5866949 A	19990202	19
9	☐	☒	US 5814883 A	19980929	16
10	☐	☒	US 5756380 A	19980526	11
11	☐	☒	US 5559306 A	19960924	6
12	☐	☒	US 5508556 A	19960416	7
13	☐	☒	US 5490324 A	19960213	15
14	☐	☒	US 5150193 A	19920922	28

	Title	Current OR	Current XRef
8	Chip scale ball grid array for integrated circuit packaging	257/778	257/678; 257/693
9	Packaged semiconductor chip	257/712	257/675; 257/700; 257/704; 257/706; 257/707; 257/717; 257/720; 257/738
10	Method for making a moisture resistant semiconductor device having an organic substrate	438/126	438/125; 438/127
11	Electronic package with improved electrical performance	174/52.4	174/35GC; 257/659
12	Leaded semiconductor device having accessible power supply pad terminals	257/691	257/698; 257/780
13	Method of making integrated circuit package having multiple bonding tiers	29/830	174/52.4; 257/686; 257/700; 438/118; 438/126
14	Resin-encapsulated semiconductor device having a particular mounting structure	257/669	257/676; 257/787

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
8		Schueller, Randolph D.	☒	☐	☐	☐	☐	☐	☐
9		Sawai, Akiyoshi et al.	☒	☐	☐	☐	☐	☐	☐
10		Berg, Howard M. et al.	☒	☐	☐	☐	☐	☐	☐
11		Mahulikar, Deepak	☒	☐	☐	☐	☐	☐	☐
12		Lin, Paul T.	☒	☐	☐	☐	☐	☐	☐
13		Newman, Keith G.	☒	☐	☐	☐	☐	☐	☐
14		Yasuhara, Toshihiro et al.	☒	☐	☐	☐	☐	☐	☐

	Image Doc. Displayed	PT
8	US 5866949	☐
9	US 5814883	☐
10	US 5756380	☐
11	US 5559306	☐
12	US 5508556	☐
13	US 5490324	☐
14	US 5150193	☐